Notice of Allowability	Application No.	Applicant(s)	
	10/501,539	ABE, KATSUMI	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/16/2004*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/16/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Nitin Patel

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Thomas G. Bilodeau on 6/8/2006.

3. The application has been amended as follows:

Claim 5 has been replaced with following amended claim 5.

A semiconductor device that performs active drive current programming, comprising: current load cells each having a current load and a current load driving circuit, which are arranged in a matrix; and a means for selecting a plurality of data lines one by one with respect to one current output from a current driver for supplying current to the respective data lines, and supplying the current output to the selected data line;

wherein the current load driving circuit in each of the current load cells includes: a means for outputting a voltage according to the current supplied from the current driver through the data line;

a means for maintaining the voltage;

a means for supplying current to the current load according to the voltage maintained; and

a means for controlling **functions of the current load of the driving circuit** according to an input control signal; and

wherein there are control lines for transmitting the control signal at least as many as data lines selectable by one current output of the current driver in one line of the semiconductor device.

REASON FOR ALLOWANCE

4. Claims 1-29 is allowed.

5. The following is an examiner's statement of reason for allowance:

Yoshiyuki (JP 020022215095 A) teaches a transistor (element 32 in fig.3) whose source is connected to a first power supply (element 38 in fig.3) while whose drain is connected to the current load (element 31 in fig.3) directly or via a switch (element 35 in fig.3); a capacitance (element 33 in fig.3) connected between the gate of the transistor (element 32 in fig.3) and the first power supply (element 38 in fig.3) or another power supply; and a switch (element 35 in fig.3) or a plurality of series-connected switches connected between the gate of the transistor and a corresponding data line.

Yamazaki et al., (US 20020079512 A1) shows a gate electrode of the switching TFT 3302 is connected to the EL display gate signal line G, one of a source region and a drain region of the switching TFT 3302 is connected to the EL display source signal line S, and the other is connected one electrode of the capacitor 3304 and to the gate electrode of the EL driver TFT 3303. The other electrode of the capacitor 3304 is connected to the electric power source line V. One of a source region and a drain region of the EL driver TFT 3303 is connected to the electric power source supply line V, and the other is connected to the EL element 3301.

The prior art fails to teach or suggest a semiconductor device that performs active drive current programming, comprising: current load cells each having a current load and a current load driving circuit, which are arranged in a matrix; and a means for selecting a plurality of data lines one by one with respect to one current output from a current driver for supplying current to the respective data lines, and supplying the current output to the selected data line; wherein the current load driving circuit in each of the current load cells includes: a transistor whose source is connected to a first power supply while whose drain is connected to the current load directly or via a switch; a capacitance connected between the gate of the transistor and the first power supply or another power supply; and a switch or a plurality of series-connected switches connected between the gate of the transistor and a corresponding data line; and wherein there are control lines for controlling the switch connected to the gate of the transistor included in each of the current load driving circuits at least as many as data lines selectable by one current output of the current driver in one line of the semiconductor device as claimed in claim 1.

The prior art fails to teach or suggest a semiconductor device that performs active drive current programming, comprising: current load cells each having a current load and a current load driving circuit, which are arranged in a matrix; and a means for selecting a plurality of data lines one by one with respect to one current output from a current driver for supplying current to the respective data lines, and supplying the current output to the selected data line; wherein the current load driving circuit in each of the current load cells includes: a transistor whose source is connected to a first power

supply while whose drain is connected to the current load directly or via a switch; a capacitance connected between the gate of the transistor and the first power supply or another power supply; and a plurality of switches connected in series between the gate of the transistor and a corresponding data line; and wherein there are control lines for controlling the switch connected to the gate of the transistor included in each of the current load driving circuits at least as many as data lines selectable by one current output of the current driver in one line of the semiconductor device; and there is a control line for controlling the switch whose one end is connected to the data line corresponding to the current load cell having the current load driving circuit in each line of the semiconductor device as claimed in claim 3.

The prior art fails to teach or suggest a semiconductor device that performs active drive current programming, comprising: current load cells each having a current load and a current load driving circuit, which are arranged in a matrix; and a means for selecting a plurality of data lines one by one with respect to one current output from a current driver for supplying current to the respective data lines, and supplying the current output to the selected data line; wherein the current load driving circuit in each of the current load cells includes: a means for outputting a voltage according to the current supplied from the current driver through the data line; a means for maintaining the voltage; a means for supplying current to the current load according to the voltage maintained; and a means for controlling the implementation of the functions according to an input control signal; and wherein there are control lines for transmitting the control signal at least as many as data lines selectable by one current output of the current

driver in one line of the semiconductor device as claimed in claim 5.

The prior art fails to teach or suggest a semiconductor device that performs active drive current programming, comprising: current load cells each having a current load and a current load driving circuit, which are arranged in a matrix; and a means for selecting a plurality of data lines one by one with respect to one current output from a current driver for supplying current to the respective data lines, and supplying the current output to the selected data line; wherein the current load driving circuit in each of the current load cells includes at least: a means for outputting a voltage according to the current supplied from the current driver through the data line; a means for maintaining the voltage; a means for supplying current to the current load according to the voltage maintained; a means for controlling whether or not to maintain the voltage according to a first control signal input into the current load cell; and a means for controlling whether or not to establish a connection between the data line and the means for outputting the voltage according to a second control signal input into the current load cell; and wherein there are control lines for transmitting the first control signal at least as many as data lines selectable by one current output of the current driver in one line of the semiconductor device; and there is a control line for transmitting the second control signal in each line of the semiconductor device as claimed in claim 6.

The prior art fails to teach or suggest a semiconductor device driving method for driving a semiconductor device that performs active drive current programming and comprises current load cells each having a current load and a current load driving circuit, which are arranged in a matrix, wherein: one current output of a current driver for

current-driving data lines is input in a selector, the selector selects the plural data lines connected respectively to the outputs of the selector one by one based on an output select signal input therein, and the current output of the current driver is supplied to the selected data line; the current load driving circuit in each of the current load cells includes: a transistor whose source is connected to a first power supply while whose drain is connected to the current load directly or via a switch for supplying current to the current load; a capacitance connected between the gate of the transistor and the first power supply or another power supply; and a switch or a plurality of series-connected switches connected between the gate of the transistor and a corresponding data line; and there are control lines for controlling the switch in the current load driving circuit at least as many as data lines selectable by one current output of the current driver in one line of the semiconductor device; the semiconductor device driving method comprising, in one horizontal period for selecting one line: a first step for passing current corresponding to the current output supplied from the current driver to the selected data line through the transistor in the current load cell by turning on the switch whose one end is connected to the gate of the transistor in the current load cell with a control signal transmitted through one of the plural control lines corresponding to the selected data line during the period while the selector selects one of the plural data lines based on the output select signal; and a second step for turning off the switch before or upon completion of the select period for the selected data line; wherein the first and second steps are performed with respect to each of the plural data lines to complete current programming for the current load cells corresponding to one line as claimed in claim 10.

The prior art fails to teach or suggest a semiconductor device driving method for driving a semiconductor device that performs active drive current programming and comprises current load cells each having a current load and a current load driving circuit, which are arranged in a matrix, wherein: one current output of a current driver for current-driving data lines is input in a selector, the selector selects the plural data lines connected respectively to the outputs of the selector one by one based on an output select signal input therein, and the current output of the current driver is supplied to the selected data line, the current load driving circuit in each of the current load cells includes: a transistor whose source is connected to a first power supply while whose drain is connected to the current load directly or via a switch for memorizing and supplying current to the current load; a capacitance connected between the gate of the transistor and the first power supply or another power supply; and a plurality of switches connected in series between the gate of the transistor and a corresponding data line; there are control lines for controlling the switch whose one end is connected to the gate of the transistor included in the current load driving circuit at least as many as data lines selectable by one output of the current driver in one line of the semiconductor device; and there is a control line for controlling the switch whose one end is connected to the data line corresponding to the current load cell having the current load driving circuit in each line of the semiconductor device; the semiconductor device driving method comprising, in one horizontal period for selecting one line: a first step for setting the respective switches whose one ends are connected to the data lines corresponding to the current load cells for one line to the on state during one horizontal period with a

control signal transmitted through the control line provided to each line; a second step for passing current corresponding to the current output supplied from the current driver to the selected data line through the transistor in the current load cell by turning on the switch whose one end is connected to the gate of the transistor in the current load cell with a control signal transmitted through one of the plural control lines corresponding to the selected data line during the period while the selector selects one of the plural data lines based on the output select signal; and a third step for turning off the switch before or upon completion of the select period for the selected data line; wherein the second and third steps are performed with respect to each of the plural data lines to complete current programming for the current load cells corresponding to one line as claimed in claim 11.

The prior art fails to teach or suggest a semiconductor device comprising: a plurality of data lines running in one direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving

circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load directly or via a third switch, the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line directly or via a second switch; there are control lines each transmitting a control signal corresponding to the first switch or the first and second switches of the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector at least as many as data lines connected to the selector; and in each of the plural current load cells, the control signal corresponding to each of the current load cells is supplied to the control terminal of the first switch or the control terminals of both the first and second switches of the current load driving circuit as claimed in claim 12.

The prior art fails to teach or suggest a semiconductor device comprising: a plurality of data lines running in one direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-

driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load directly or via a third switch, the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line via a second switch; there are at least control lines each transmitting a control signal corresponding to the first switch of the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector; there is a control line for transmitting a common control signal corresponding to the second switch of the current load driving circuit in each of the current load cells; the control signal corresponding to each of the current load cells is supplied to the control terminal of the first switch of the current load driving circuit in the current load cell; and the common control signal is supplied to the control terminal of the second switch of the current load driving circuit in the current load cell as claimed in claim 13.

The prior art fails to teach or suggest a semiconductor device driving method for driving a semiconductor device comprising: a plurality of data lines running in one direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load, the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line directly or via a second switch; there are control lines each transmitting a control signal corresponding to each of the current load cells connected respectively to the data lines connected to the selector; and in each of the plural current load cells, the

control terminal of the first switch or the control terminals of both the first and second switches of the current load driving circuit are supplied with a control signal through the control line set correspondingly to each of the current load cells; the semiconductor device driving method, wherein one cycle is divided into a number of driving periods corresponding to the plural current load cells connected respectively to the plural data lines connected to the driver via the selector, comprising the steps of: (a) selecting one corresponding data line from the plural data lines by the selector based on the output select signal during each driving period corresponding to each of the plural current load cells; (b) passing current corresponding to the current output supplied from the driver to the data line through the first MOS transistor in the current load cell by turning on the first switch or the first and second switches in the current load cell with a control signal transmitted through one of the control lines for the current load cell corresponding to the data line selected by the selector; and (c) turning off the first switch or the first and second switches in the current load cell with a control signal transmitted through the control line for the current load cell corresponding to the data line selected at step (a) before or at the time the selector proceeds to select the next data line based on the output select signal; wherein the operating steps (a) and (b) are performed with respect to each of the plural data lines connected to the driver via the selector to complete current programming for the current load cells corresponding to one cycle as claimed in claim 22.

The prior art fails to teach or suggest a semiconductor device driving method for driving a semiconductor device comprising: a plurality of data lines running in one

direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load, the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line via a second switch; there are control lines each transmitting a control signal corresponding to the first switch of the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector; there is a common control line for transmitting a common control signal corresponding to the second switch of the current load driving circuit in each of the current load cells; the

control signal being individual to each of the current load cells is supplied to the control terminal of the first switch of the current load driving circuit in the current load cell; and the common control signal is supplied to the control terminal of the second switch of the current load driving circuit in the current load cell; the semiconductor device driving method, wherein one cycle is divided into a number of driving periods corresponding to the plural current load cells connected respectively to the plural data lines connected to the driver via the selector, and the second switch in the current load cell is on during one cycle according to the common control signal, comprising the steps of: (a) selecting one corresponding data line from the plural data lines by the selector based on the output select signal during each driving period corresponding to each of the plural current load cells; (b) passing current corresponding to the current output supplied from the driver to the data line through the first MOS transistor in the current load cell by turning on the first switch in the current load cell with a control signal transmitted through one of the control lines for the current load cell corresponding to the data line selected by the selector; and (c) turning off the first switch with a control signal transmitted through the control line for the current load cell corresponding to the data line selected at step (a) before or at the time the selector proceeds to select the next data line based on the output select signal; wherein the operating steps (a) and (b) are performed with respect to each of the plural data lines connected to the driver via the selector to complete current programming for the current load cells corresponding to one cycle as claimed in claim 23.

The prior art fails to teach or suggest a semiconductor device driving method for

driving a semiconductor device comprising: a plurality of data lines running in one direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load via a switch (referred to as "third switch"), the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line directly or via a second switch; there are control lines each transmitting a control signal corresponding to each of the current load cells connected respectively to the data lines connected to the selector; in each of the plural current load cells, the control terminal of the first switch of the current

load driving circuit or the control terminals of both the first and second switches are supplied with the control signal through the control line corresponding to each of the current load cells; a fourth switch is placed between a contact node connecting one end of the current load with the third switch and the second power supply; and there are a common control line connected to the control terminal of the third switch and a common control line connected to the control terminal of the fourth switch for the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector; the semiconductor device driving method, wherein one cycle is divided into a number of driving periods corresponding to the plural current load cells connected respectively to the plural data lines connected to the driver via the selector, comprising the steps of: (a) selecting one corresponding data line from the plural data lines by the selector based on the output select signal during each driving period corresponding to each of the plural current load cells; (b) turning on the first switch or the first and second switches in the current load cell with one of control signals for the current load cell corresponding to the data line selected by the selector, and setting the third switch to the off state with a control signal transmitted through the common control line so as to set the terminal voltage of the capacitance connected to the gate of the first MOS transistor to a voltage corresponding to the current output supplied from the driver to the data line; (c) turning off the first switch or the first and second switches in the current load cell with a control signal for the current load cell corresponding to the data line selected at step (a) before or at the time the selector proceeds to select the next data line based on the output select signal; and (d) after the operating steps (a) and (b)

are performed with respect to each of the plural data lines connected to the driver via the selector to set a current for the first MOS transistor of the respective current load cells corresponding to one cycle, turning on the third switch subsequently to the previous cycle so that the drain current of the first MOS transistor in the current load cell is supplied to the current load cell as claimed in claim 25.

The prior art fails to teach or suggest a semiconductor device driving method for driving a semiconductor device comprising: a plurality of data lines running in one direction on a substrate; a plurality of control lines running in a direction perpendicular to the data lines; a plurality of current load cells each of which is set at the intersection of the respective data lines and control lines, and includes a current load and a current load driving circuit for driving the current load; and a selector having an input terminal to which one current output from a driver for current-driving the data lines is input, and a plurality of output terminals connected to the plural data lines, respectively; wherein: the selector selects one of the plural data lines according to an output select signal input therein, and supplies the current output from the driver to the selected data line; the plural data lines connected to the selector are connected to their corresponding current load cells, respectively; the current load driving circuit in each of the current load cells includes: a first MOS transistor whose source is connected to a first power supply while whose drain is connected to one end of the current load via a switch (referred to as "third switch"), the other end of the current load being connected to a second power supply; a capacitance whose one end is connected to the gate of the first MOS transistor while whose the other end is connected to the first power supply or another

power supply; and a first switch whose one end is connected to a contact node between the gate of the first MOS transistor and one end of the capacitance while whose the other end is connected to a corresponding data line via a second switch; there are control lines each transmitting a control signal corresponding to the first switch of the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector; there is a common control line corresponding to the second switch of the current load driving circuit in each of the current load cells; the control terminal of the first switch of the current load driving circuit in the current load cell is supplied with the control signal through the control line corresponding to each of the current load cells; the control terminal of the second switch of the current load driving circuit in the current load cell is supplied with a control signal through the common control line; a fourth switch is placed between a contact node connecting one end of the current load with the third switch and the second power supply; and there are a common control line connected to the control terminal of the third switch and a common control line connected to the control terminal of the fourth switch for the current load driving circuit in each of the current load cells connected respectively to the data lines connected to the selector; the semiconductor device driving method, wherein one cycle is divided into a number of driving periods corresponding to the plural current load cells connected respectively to the plural data lines connected to the driver via the selector, and the second switch in the current load cell is on while the third switch is off during one cycle according to the control signal transmitted through the common control line, comprising the steps of: (a) selecting one corresponding data line from the plural

data lines by the selector based on the output select signal during each driving period corresponding to each of the plural current load cells; (b) turning on the first switch in the current load cell with one of control signals for the current load cell corresponding to the data line selected by the selector so as to set the terminal voltage of the capacitance connected to the gate of the first MOS transistor to a voltage corresponding to the current output supplied from the driver to the data line; (c) turning off the first switch with a control signal for the current load cell corresponding to the data line selected at step (a) before or at the time the selector proceeds to select the next data line based on the output select signal; and (d) after the operating steps (a) and (b) are performed with respect to each of the plural data lines connected to the driver via the selector to set a current for the first MOS transistor of the respective current load cells corresponding to one cycle, turning on the third switch subsequently to the previous cycle so that the drain current of the first MOS transistor in the current load cell is supplied to the current load cell as claimed in claim 26.

The prior art fails to teach or suggest a semiconductor device comprising: a plurality of data lines running in one direction; a plurality of control lines running in a direction perpendicular to the data lines; and a matrix of current load cells each of which is set at the intersection of the respective data lines and control lines; wherein each of the current load cells includes: a current load; and a current load driving circuit for driving the current load, having: a transistor connected in series with the current load between first and second power supplies; a capacitance connected between the control terminal of the transistor and the first power supply; and at least one switch connected

between the control terminal of the transistor and a corresponding data line; and wherein there are control lines for controlling the switch at least as many as data lines selectable by one current output of a current driver in one line of the semiconductor device; and one current output of the current driver is connected to the plural data lines via a selector, and the plural data lines connected to one current output of the current driver via the selector and at least one switch of each of the current load cells corresponding to the respective data lines are drive-controlled in a time division manner during one horizontal period as claimed in claim 29.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Examiner
Art Unit 2629